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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/974,056	Applicant(s) LEE ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- *The MAILING DATE of this communication appears on th cov r sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardee (5,389,842) in view of Igarashi (4,656,491) or Steudel (3,712,995). Hardee teaches in figure 2 and related text an ESD protection component, comprising: at least two MOS field effect transistors 26, 42 (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer 20 having a second conductivity type; a first well 22 having a first conductivity type, formed on the first semiconductive layer, comprising: a connecting area 22, formed between the MOS FETs; two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and a first doping area 34 of the second conductivity type, formed in the connecting area, wherein the first well is separated from the drains of the MOS FETs, wherein each of the MOS FETs has a source region of the first conductivity type coupled to a power rail, and wherein the first doping region and each of the MOS FETs

has a drain region of the first conductivity type coupled to a pad, and two drains of the first conductivity type.

Hardee does not teach a first well comprising two parallel extension areas formed perpendicular to the gates of the MOS FETs.

Igarashi teaches in figures 2 and 5 a first well 12 and 31 comprising two parallel extension areas, respectively.

Steudel teaches I figure 4 a first well 69 comprising two parallel extension areas.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first well comprising two parallel extension areas in Hardee's device, in order to reduce the contact resistance of the device by enlarging the contact area of the first well.

Regarding the claimed limitation of extension areas formed perpendicular to the gates of the MOS FETs, the extension areas are formed in the semiconductor substrate and thus are perpendicular to the gates of the MOS FETs.

Regarding claim 6, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the pad to the first well through the extension areas in order to reduce the contact resistance of the device by connecting the enlarged contact area of the first well to the pad.

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hardee, Igarashi and Steudel, as applied to claim 1 above, and further in view of Ker et al. (6,072,219).

Hardee, Igarashi and Steudel teach substantially the entire claimed structure, as applied to claim 1 above, except using a guard ring of the second conductivity type, wherein a first conductive layer is connected to a power supply through the guarding ring.

Ker et al. teach in figure 8 a guard ring P+ of the second conductivity type, wherein a first conductive layer (see figure 7) is connected to a power supply through the guarding ring.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a guard ring of the second conductivity type, wherein a first conductive layer is connected to a power supply through the guarding ring in prior art's device, in order to provide better electrical isolation for the device.

Response to Arguments

4. Applicant argues that Hardee does not teach that each of the MOS FET's source region is coupled to a power rail, the first well is coupled to a pad through the extension

areas, the first doping region is coupled to a pad, and each of the MOS FET's drain regions is coupled to a pad, as recited in claims 5-9, respectively.

Hardee teaches that each of the MOS FET's source regions is coupled to a power rail, the first well is coupled to a pad through the extension areas, the first doping region is coupled to a pad, and each of the MOS FET's drain regions is coupled to a pad, as recited in claims 5-9, respectively, for the following reasons. Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See, e.g., In re Zletz, 893 F.2d 319, 321 - 22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow . ."). The term 'couple' is defined as bringing (two electric circuits) into such close proximity as to permit mutual influence. That is, each of the MOS FET's source regions should have an electrical connection to the power rail, the first well should have an electrical connection to the pad, the first doping region should have an electrical connection to the pad, and each of the MOS FET's drain regions should have an electrical connection to the pad, in order for these elements to be coupled together. Hardee teaches that each of the MOS FET's source regions has an electrical connection to the power rail, the first well has an electrical connection to the pad, the first doping region has an electrical connection to the pad, and each of the MOS FET's drain regions has an electrical connection to the pad. Therefore, Hardee teaches that each of the MOS FET's source regions is coupled to a

power rail, the first well is coupled to a pad, the first doping region is coupled to a pad, and each of the MOS FET's drain regions is coupled to a pad, as claimed. Note that the broad recitation of the claims does not require that each of the MOS FET's source regions is directly connected to a power rail, the first well is directly connected to a pad through the extension areas, the first doping region is directly connected to a pad, and each of the MOS FET's drain regions is directly connected to a pad.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
July 9, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800